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(71) Applicant: MOTOROLA, INC. [US/US]; 1303 E. Algonquin Road, Schaumburg, IL 60196 (US).

(72) Inventors: THOMPSON, Kenneth, R. ; 11461 N.W. 35 Place, Sunrise, FL 33323 (US). BANERJI, Kingshuk ; 810 N.W. 98 Avenue Sunrise, Plantation, FL 33324 (US). MULLEN, William, B., III ; 9651 S.W. 12 Court, Boca Raton, FL 33428 (US).

(74) Agents: NICHOLS, Daniel, K. et al.; Motorola, Inc., Intellectual Property Dept., 8000 West Sunrise Blvd., Ft. Lauderdale, FL 33322 (US).

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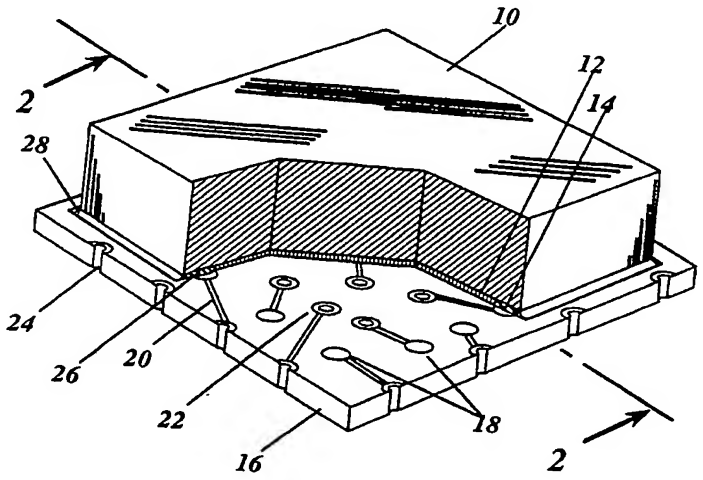

(57) Abstract

An integrated circuit chip carrier assembly, comprising a semiconductor device (10) having interconnection pads (14) disposed on an active surface (12) of the device. The device (10) is attached by means of electrically conducting bumps (26) to a circuitry pattern (18) on a first side of a circuit carrying substrate (16). The substrate is typically an aramid reinforced organic resin, such as epoxy. The circuitry (18, 20) is electrically connected by conductive through-holes (22) to an array of solder pads on a second side of the substrate. Some or all of the through-holes (22) are covered by the device. The overall length and width of the circuit carrying substrate (16) are each a maximum of about 0.15 inches greater than the equivalent dimensions of the device (10), creating a carrier that is only slightly larger than the semiconductor device itself.

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PATENT APPLICATION

INTEGRATED CIRCUIT CHIP CARRIER

Technical Field

This invention relates generally to the field of integrated circuits and most particularly to a reduced size integrated circuit chip carrier.

Background

The demand for manufacturing electrical assemblies with greater densities and smaller package size requires devising techniques to efficiently utilize the available area on a printed circuit board. One such technique is to directly bond the integrated circuit chip to corresponding contact points on a printed circuit board, thereby eliminating the necessity of using a chip carrier with a conventional ceramic or plastic cover or encapsulating the integrated circuit chip. The most popular method of directly bonding a chip to a circuit board is known as chip-on-board (COB). In chip-on-board, the integrated circuit is mounted directly on the circuit board and either wire bonded to the circuit board or bonded using TAB technology. This technique has been widely used in manufacturing of watches and other small electronic products. However, the integrated circuit chip is brittle and fragile and subject to stress and breakage if the circuit board is bent, vibrated or exposed to wide variations in temperature. Accordingly, in many applications such as two-way radios and other portable communication devices, where the electrical assembly is subject to vibration and severe environmental disturbances, direct connections between the integrated circuit chip and the circuit board are not desirable and can cause reliability problems.

Conventional ways of protecting and packaging the integrated circuit, such as chip carriers or transfer molded integrated circuit devices, provide a buffer substrate or mounting scheme between the integrated circuit and the circuit board, thereby reducing or eliminating the stress imparted to the chip during mechanical and thermal excursions. There are numerous drawbacks to the use of these types of chip carriers. Chip carriers are larger than the integrated circuit and typically require two to three times the area on the circuit board as the integrated circuit. The finished package is typically expensive and not repairable. The inability to repair a rather expensive package becomes a liability in electrical testing.

In chip-on-board technology, the density of lines and spaces required on the circuit board is extremely high, thereby creating a very complex printed circuit board with fine lines and spaces that is very expensive to manufacture. The use of chip carriers allows one to incorporate printed circuit boards with less stringent line and space requirements, thereby reducing the cost of the printed circuit board. This cost reduction comes at the expense of using a larger chip carrier package which is more expensive and also has a greater height.

In chip-on-board technology, the semiconductor device is attached to the substrate by means of the control-collapse-chip-connection (known as C4). Typically, in order to achieve high yields and reliability in making a C4 connection, a clean room environment must be utilized during this process. One can easily see that the C4 process is not suitable for a normal manufacturing assembly environment where components are mounted onto circuit boards.

Clearly, a need exists for an integrated circuit package that can solve the problems of mechanical and thermal excursions, reduced size, utilize less dense (lower cost) printed circuit boards, provide chip carriers that can be electrically tested prior to assembly to the main circuit board, and does not require a clean room environment for assembly to the main circuit board.

Summary of the Invention

Briefly, according to the invention, there is provided an integrated circuit device assembly comprising a semiconductor device with

interconnecting pads arranged on an active surface of the device. The device is bonded to a substrate by attaching the device face down to corresponding circuit pads on the substrate. The circuit pads of the substrate are connected to solder pads on the opposite side of the substrate by conductive thru-holes. The integrated circuit device is connected to the substrate by electrically conductive bumps between the device pads and the substrate pads such that the device covers at least some of the conductive thru-holes on the substrate.

In another aspect of the invention, the gap between the device and the substrate may be filled with an organic coupling agent such as an epoxy resin.

Brief Description of the Drawings

FIG. 1 is an isometric cut-away view of the integrated circuit chip carrier in accordance with the invention.

FIG. 2 is a cross section of the chip carrier of FIG. 1 through section 2-2.

FIG. 3 is a cross section of an alternate embodiment of the chip carrier of FIG. 1 through section 2-2.

FIG. 4 is a cross section of an alternate embodiment of the chip carrier of FIG. 1 through section 2-2.

Detailed Description of the Preferred Embodiment

Referring now to FIG. 1, an integrated circuit or semiconductor device 10 contains an active surface 12 having interconnection pads 14 arranged in a configuration near the perimeter of the device. A circuit carrying substrate 16 has an array of interconnection pads 18 that correspond to the interconnect pads 14 of the device. The substrate material is typically a printed circuit board. Circuit boards made from materials with low expansion coefficients are preferred (between about 6 and about 18 in/in/°Cx10^{-6}). One example of a useful material is Thermount E-215/CE laminate from the DuPont Corporation of Wilmington, Delaware. This laminate is an epoxy resin reinforced with aramid fiber. Other types of organic resins such as polyesters, polyamides, polyimides, and modifications or blends of these resins may also be employed in conjunction with the aramid reinforcements. Other

types of substrates such as alumina ceramic, beryllium oxide, or aluminum nitride may also be effectively employed. In addition, the substrate 16 also contains other circuitry 20 that interconnects the pads to conductive thru-holes or vias 22 in the substrate. The circuitry 20 may also be connected to semicircular conductive thru-holes 24 on the perimeter of the substrate.

By utilizing an array of conductive thru-holes on the perimeter and the interior of the substrate, each of the integrated circuit interconnect pads 14 may be routed to a corresponding solder pad on the bottom of the substrate 16. In so doing, the lines and spaces required for the solder pads are much larger than those on the integrated circuit device since the entire surface of the substrate may be used. For example, spaces between interconnect pads on an integrated circuit device are typically 0.004 inches. By interconnecting the device to a substrate in this manner, the spacings between the solder pads on the bottom of the substrate may be as great as 0.030 inches. The solder pad diameters may be as great as 0.030 inches as opposed to 0.004 inches on the device interconnect pads.

The semiconductor device 10 is attached to the substrate by facing the active surface 12 of the device 10 toward the upper surface of the substrate 16. Interconnection of the device to the substrate is provided by means of conductive bumps 26 between the pads 14 of the device and the circuitry 18 of the substrate. These bumps may typically be made from solder or be thermocompression bonds, conductive epoxy, or conductive elastomer. If they are made from solder, the device is attached to the substrate by means of the control-collapse-chip-connection (C4). This type of connection is well known to those skilled in the art and has been utilized to achieve high-density circuitry. Typically, in order to achieve high yields and reliability in making a C4 connection, a clean room environment must be utilized and therefore the C4 process is most suitably employed early in the packaging process where the environment can be controlled. It should be appreciated that the chip carrier, in accordance with the present invention once completed, does not require a clean room environment in order to be attached to a main circuit board. The COB process, on the other hand, requires cleanroom conditions for assembly to the main circuit board.

After the integrated circuit is attached to the substrate, an organic coupling agent 28 may be applied in the gap between the integrated circuit and the substrate. This coupling agent may be, for example, a rigid adhesive such as an epoxy or a softer material such as a silicone. An example of a suitable coupling agent is Hysol FP 4510, an epoxy from the Dexter Corporation of Industry, California. The coupling agent serves to provide additional mechanical bonding between the device and the substrate and also serves as a stress relieving member. The third function of the coupling agent is to environmentally protect the active surface of the device and the interconnections. Depending on the application, the coupling agent may cover the entire gap between the device and the substrate or may only cover a portion of the active surface of the device.

Referring now to FIG. 2, it can be seen that the integrated circuit 10 lies over some of the conductive thru-holes 22. Each of the conductive thru-holes 22 connects to a solder pad 23 on the bottom side of the substrate 16. The organic coupling agent or underfill material 28 fills the gap between the device 10 and the substrate 16. The interconnect pads 14 of the device 10 are connected to the circuitry pads 18 of the substrate by means of a metallic bump 26. As can be seen in FIGS. 1 and 2, the overall size of the substrate 16 is only slightly larger than the overall size of the integrated circuit 10. Typically, the length and width of the substrate is no greater than 0.15 inches greater than the length and width of the device and may be as small as the device itself in some cases. Typically, the substrate is 0.025 to 0.1 inches greater than the largest dimension of the device. The assembled integrated circuit chip carrier may now be electrically tested with conventional testing equipment, without having to resort to expensive and complex semiconductor testing equipment. Since the carrier is tested at a package level, the testing regime can be more thorough, and does not require the complexity and miniaturization necessary for testing at the wafer level.

The assembly may now be placed onto a printed circuit board 25 by any number of interconnection schemes. For example, the integrated circuit assembly may be attached to the circuit board by solder joints as in the C5 process (controlled collapse chip carrier connection) or it may

be attached using elastomeric interconnects or hot-melt adhesive interconnects. In the case of the C5 connections, solder joints 27 are achieved by reflowing solder balls between the assembly and the circuit board.

Referring to FIG. 3, an alternate embodiment of the invention comprises attaching the semiconductor device 10 to a substrate 36 containing circuitry patterns 18 on one side only. The device 10 is directly attached via solder bumps 26 to the circuitry pattern on the top side of the substrate 36 to create a chip carrier assembly. The circuitry pattern extends to a hole 22 in the substrate, and may terminate in an annular ring around the hole or may cover the hole entirely so as to tent the hole. The assembly may contain the above referenced organic coupling agent 28 if desired. In order to connect the assembly to a printed circuit board 25 (PCB), the carrier is soldered to the PCB using additional, usually larger, solder bumps 37. The solder bumps 37 are soldered to the circuitry pattern 18 by forming the bumps in the substrate hole 32 so that the solder 37 connects to the back side of the circuitry pattern 18.

In a further embodiment of the invention illustrated by way of FIG. 4, a semiconductor device 10 is attached to a substrate 46 having a circuitry pattern 48 on the back side of the substrate. The device is connected to the back side of the circuitry pattern via a series of solder bumps 46 that extend through a hole 42 in the substrate to create a chip carrier assembly. As in previous examples, the assembly may contain the above referenced organic coupling agent 28 if desired. In order to connect the assembly to a printed circuit board 25 , the carrier is soldered to the PCB using additional, usually larger, solder bumps 47. The solder bumps 47 are soldered to the circuitry pattern 48 and the PCB 25 using, for example, a C5 process.

A package created in accordance with the invention provides numerous advantages, amongst which are: a package with a smaller footprint than conventional chip carrier packages, a package with a footprint only slightly larger than the actual size of the integrated circuit itself, a package with significantly reduced height (only slightly greater than the height of the integrated circuit), a package that may be easily tested prior to assembly to a main circuit board, and a package that does

not require clean room environments for assembling an integrated circuit to a main circuit board. The present invention satisfies a long-existing need for an improved integrated circuit chip carrier that is smaller is size, more reliable, lower cost, easier to manufacture, and is electrically testable. It will be apparent from the foregoing that while particular forms of the invention have been illustrated and described, various modifications can be made without departing from the spirit and the scope of the invention. The examples shown in FIG. 1 and FIG. 2 herein, while illustrative, are not meant to be considered limiting and other configurations of the present invention may be envisioned to fall within the scope of the invention. Accordingly, it is not intended that the invention be limited except as by the appended claims.

What is claimed is:

Claims

1. A semiconductor device assembly, comprising:

a circuit carrying substrate having a length and a width, a circuitry pattern on a first side and an array of solder pads spaced a first distance apart on an opposite side, the circuitry pattern being electrically connected by means of plated through holes to the array of solder pads, and;

a semiconductor device having a length and a width and a first side comprising an active surface, interconnection pads spaced a second distance apart, disposed on a perimeter of the active surface, the second distance being less than the first distance, and electrically conducting bumps on the interconnection pads;

the device being attached by means of the electrically conducting bumps to the circuitry pattern, at least some of the plated through holes being covered by the active surface of the device, and the length and width of the circuit carrying substrate each being a maximum of about 0.1 inches greater than the length and width of the device.

2. The semiconductor device of claim 1, wherein an organic coupling agent is disposed between the device and the substrate, covering at least a portion of the active surface.

3. The semiconductor device of claim 1, wherein the device is directly connected to a circuitry pattern on the first side of the circuit carrying substrate, said substrate having an unplated hole containing a solder bump connected to the circuitry pattern and extending through the hole and beyond the plane of the opposite side of the substrate.

4. A semiconductor device assembly, comprising:

a semiconductor device having interconnection pads disposed on a perimeter of an active surface of the device;

a circuit carrying substrate having two opposed sides, a first side having a circuitry pattern substantially corresponding to the semiconductor device interconnection pads, and a second side having a plurality of solder pads that are electrically connected to the circuitry pattern of the first side by plated through holes, the spacing between the plurality of solder pads being greater than the spacing between the device interconnection pads, at least some of the plated through holes being disposed in an area under the device, and the length and width of the circuit carrying substrate each being a maximum of about 0.1 inches greater than the length and width of the device;

means for electrically and mechanically coupling the device to the circuitry pattern, comprising bumps of electrically conducting material between the interconnection pads of the device and the circuitry pattern; and

an organic coupling agent disposed between the device and the substrate, covering at least a portion of the active surface.

5. The semiconductor device of claim 4, wherein the plurality of solder pads are arranged in an array.

6. The semiconductor device of claim 4, wherein the bumps comprise solder.

7. A semiconductor device assembly, comprising:

a semiconductor device having interconnection pads disposed on a perimeter of an active surface of the device;

a reinforced organic substrate having two opposed sides, a first side having an array of solder pads, the spacing between the individual solder pads being greater than the spacing between the individual device interconnection pads, and the substrate having through holes disposed in a pattern corresponding to the semiconductor device interconnection pads ;

means for electrically and mechanically coupling the device to the solder pads , comprising electrically conducting material between the device interconnection pads and the solder pads;

an epoxy resin disposed between the device and the substrate, covering at least a portion of the active surface; and

said semiconductor device mounted with the active surface facing a second opposed side of the substrate, the electrically conducting material coupling the device interconnection pads to the array of solder pads by extending through the substrate holes.

8. The semiconductor device of claim 7, wherein the bumps comprise solder.

9. The semiconductor device of claim 7, wherein the length and width of the circuit carrying substrate are each a maximum of about 0.1 inches greater than the length and width of the device.

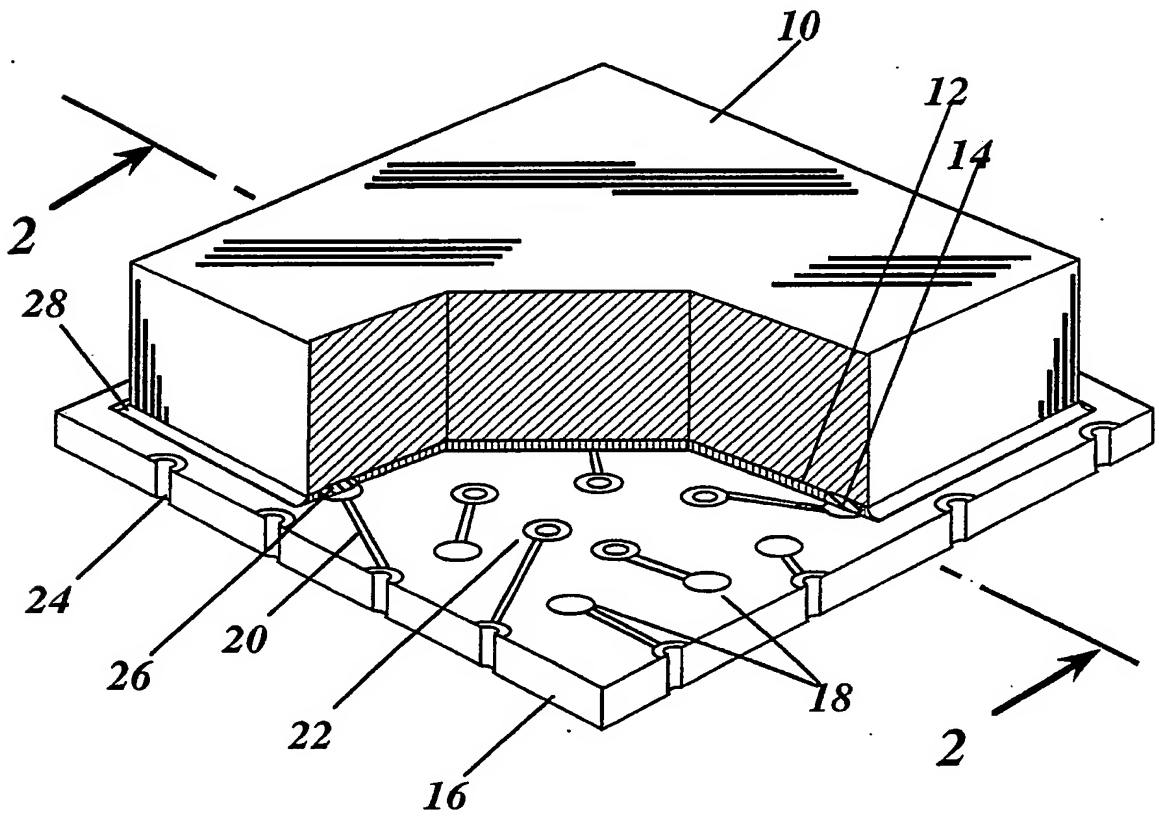

FIG. 1

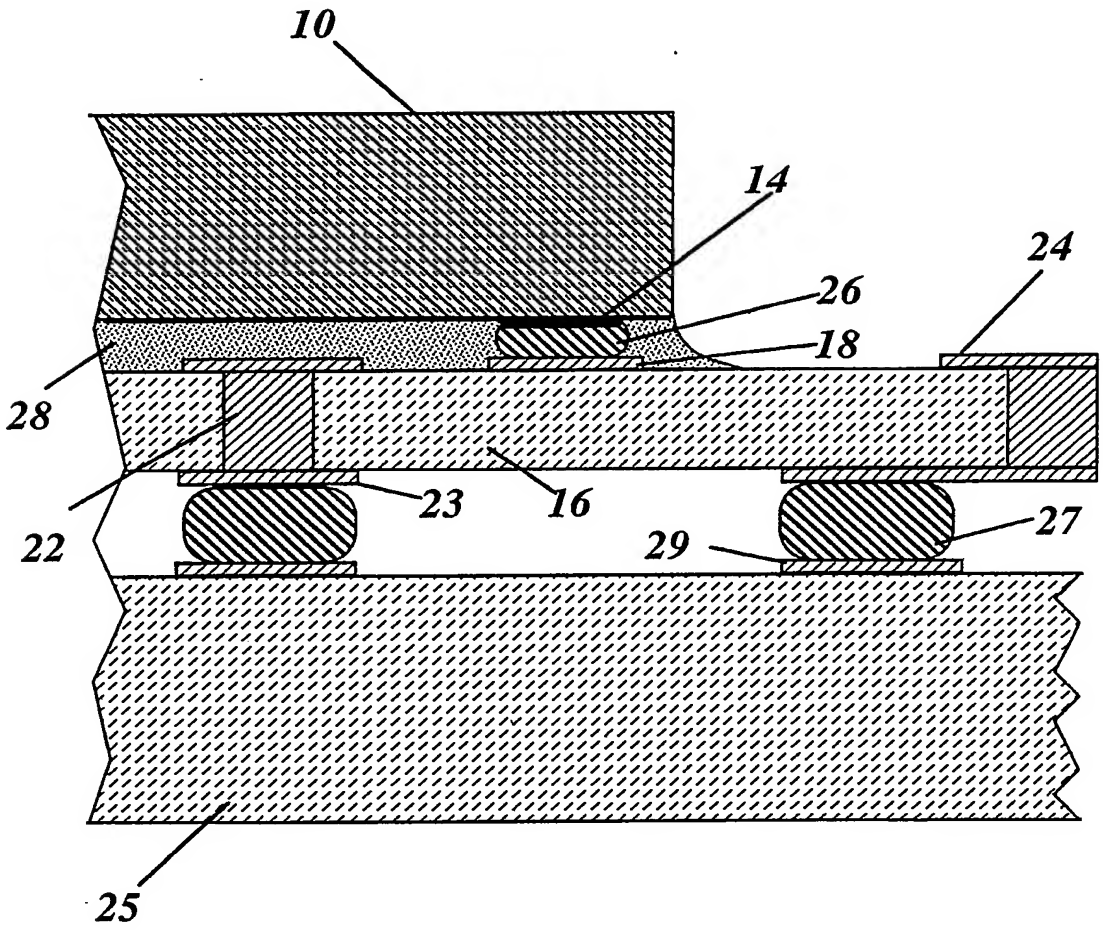

FIG. 2

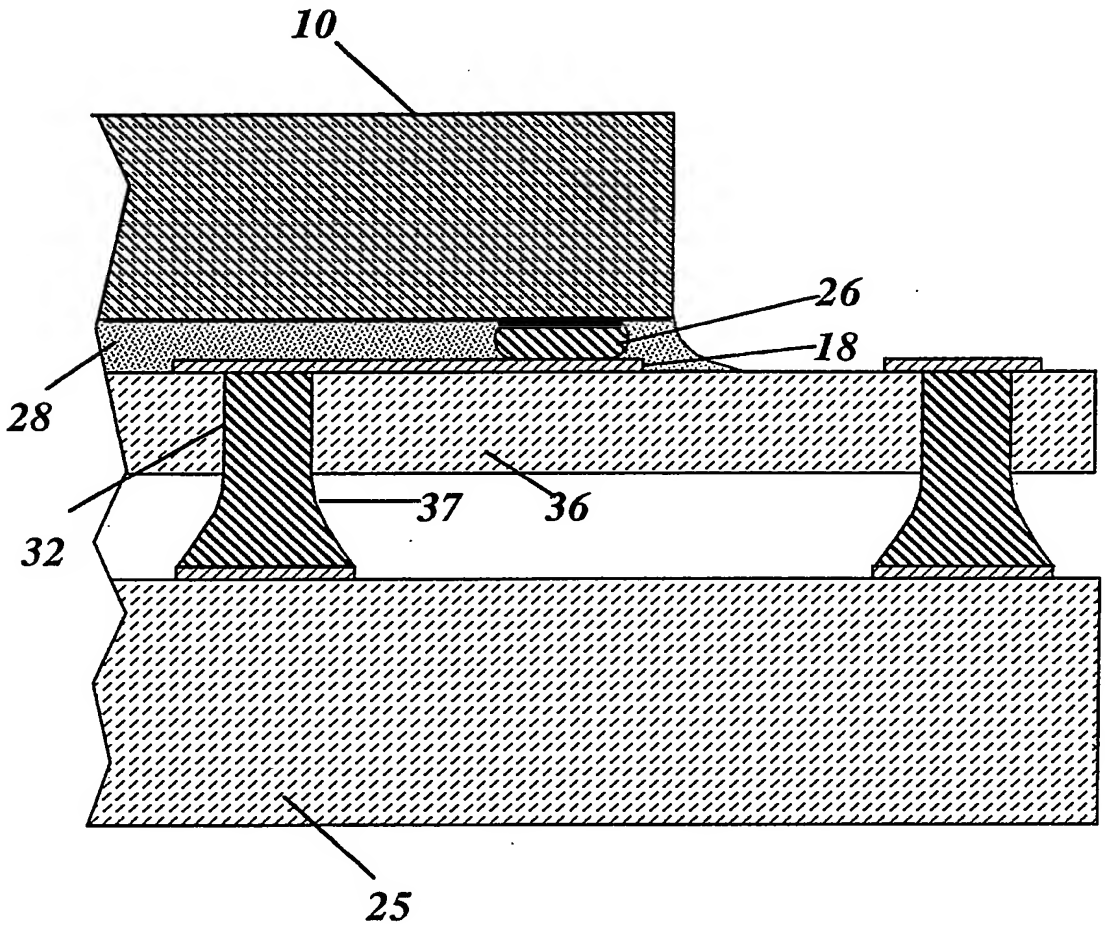

FIG. 3

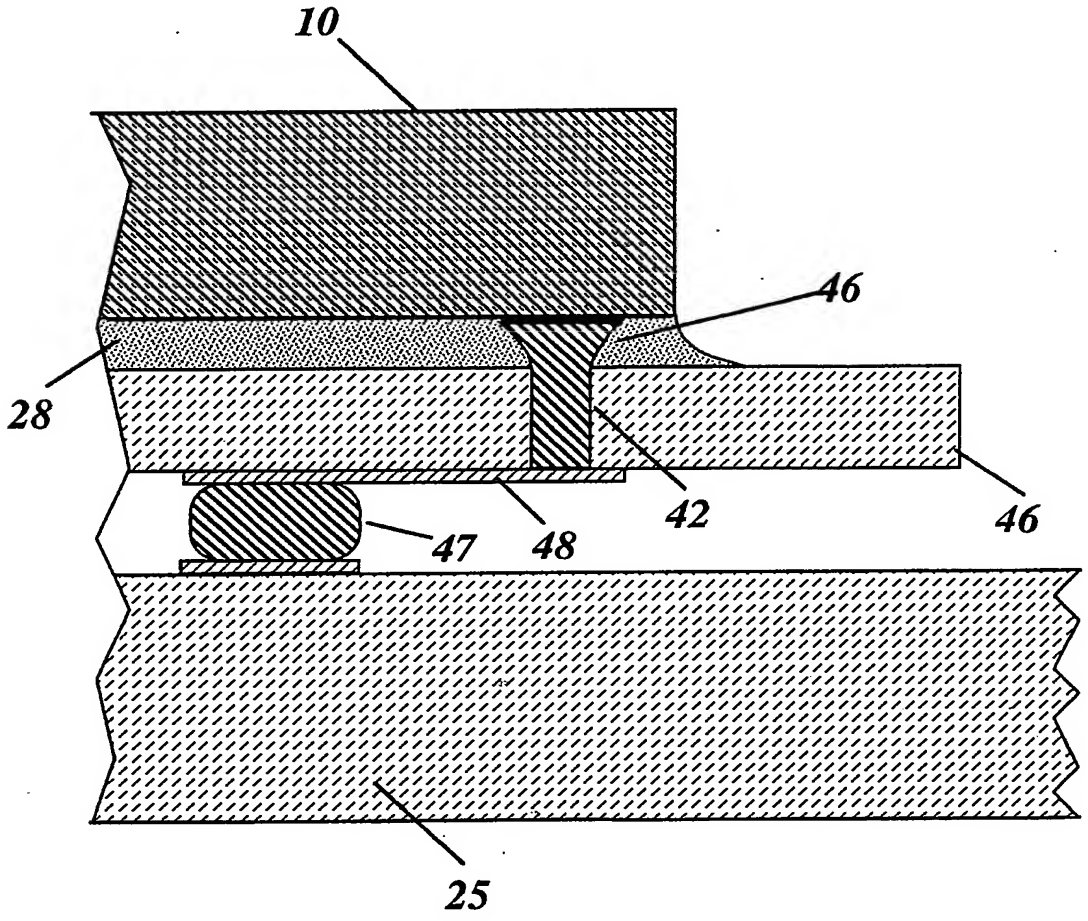

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
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A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H01L 23/02, 23/12
US CL :357/74, 80

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : H01L 23/48, 23/16
174/261; 361/400, 414; 357/75

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US, A, 4,893,172 (Matsumoto et al.) 9 January 1990, Note Figures 1b & 2a	1, 7, 8
Y	US, A, 4,963,414 (LeVasseur et al.) 16 October 1990, Note column 7, line 5.	1, 5
Y	US, A, 4,821,142 (Ushifusa et al.) 11 April 1989, Note Figure 1.	1-4, 7, 9 10, 12 to 16
Y	JP, A 59-9441 (Fujii) 31 May 1984 Note Abstract	1 to 4, 7, 9 10, 12 to 16
Y	JP, A, 61-279164 (Asano) 09 December 1986 Note Fig. 5.	1, 8

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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